Mini-EUSO photodetector module data processing system

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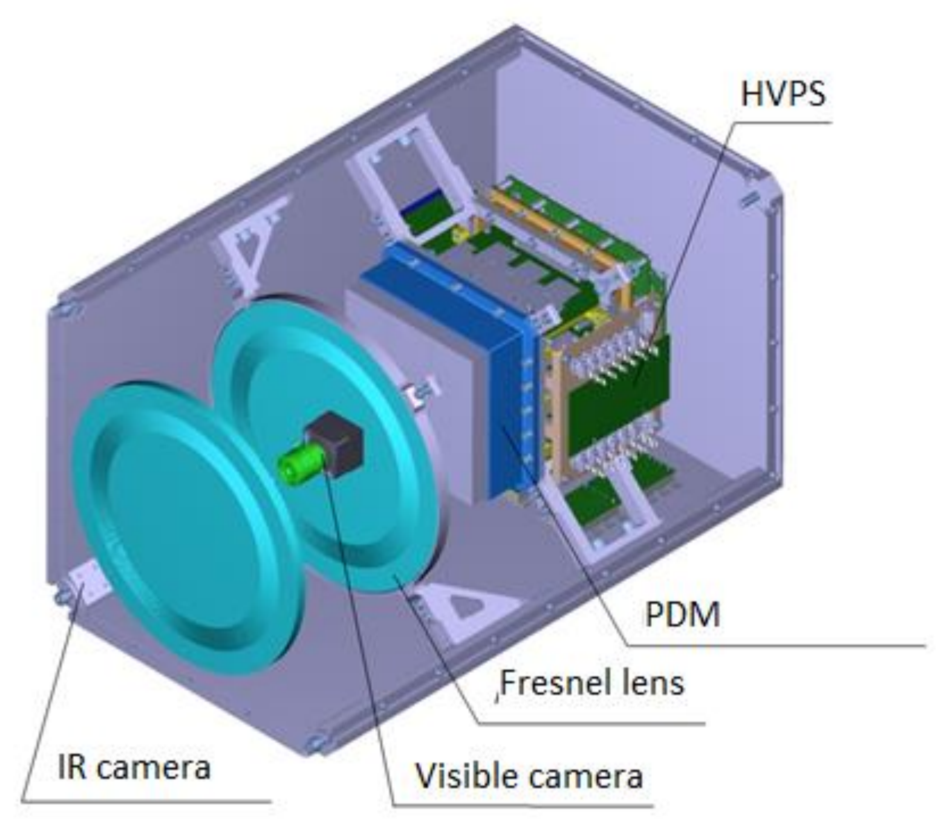
The Mini-EUSO telescope is designed for the measurement and mapping of the UV night-time emissions from the Earth and is being developed by the JEM-EUSO Collaboration as a pathfinder for the detection of extreme energy cosmic rays (EECRs, those with energies >50 EeV, 1 EeV = 10^{18} eV.) from space such as KLYPVE-EUSO on the Russian Segment of the International Space Station (ISS) and JEM-EUSO.
The Mini-EUSO mission is a joint project between Italy and Russia, was selected by the Italian Space Agency (ASI) and is supported by the National Institute of Nuclear Physics (INFN); then, under the name ``UV atmosphere'', it was approved by the Russian Space Agency Roscosmos and included in the long-term program of space experiments on the ISS. The launch of Mini-EUSO is programmed from late 2017 to early 2018.

Mini-EUSO telescope

The detector is a wide field of view telescope composed of two Fresnel lens optical system of 25 cm diameter, the photo detector module (PDM) placed in a focal plane, consisting of 36 Hamamatsu Multi Anode Photo Multiplier Tubes (MAPMTs), ancillary detectors (visible and near infra-red cameras). In the left panel of fig. 1 the 3D model of Mini-EUSO is shown.
The front-end electronics is based on the ASIC (SPACIROC3) and boards developed for the JEM-EUSO, central processor unit (CPU) is a standard PCIe/104 form factor single board computer. PDM data processing (PDM DP) system is designed specifically for the Mini-EUSO



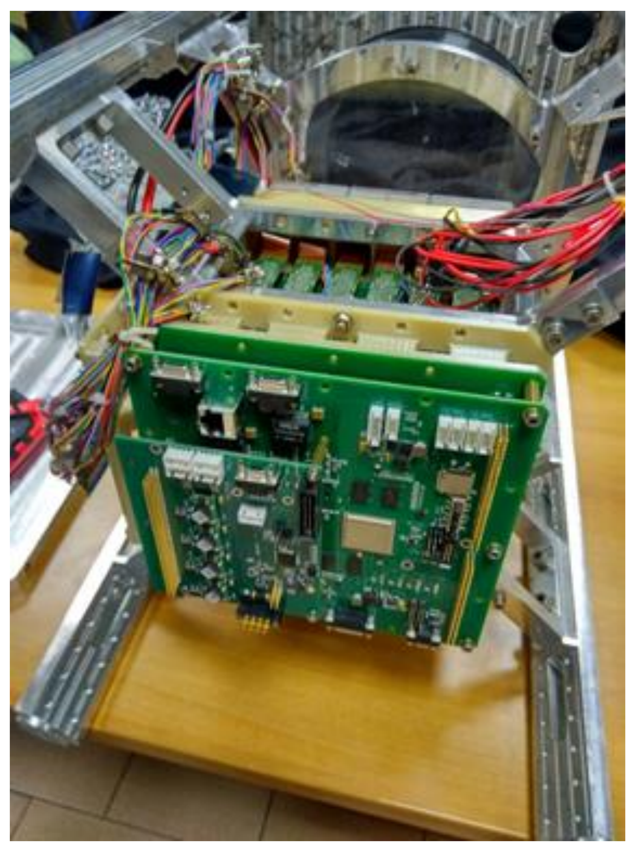


Fig.1. Left panel: The Mini-EUSO instrument 3D model. Right panel: the PDM-DP boards in the Mini-EUSO engineering model during tests.

PDM-DP functionality, multi-level trigger

The PDM DP performs the data gathering from photo detectors through SPACIROCs chips, the data preprocessing for detecting events (trigger algorithms) and the recording corresponding data fragments to the storage device. Also the PDM DP performs SPACIROC chips slow control configuration (i.e. setting the gains and analog voltage thresholds) and controls high voltage power supply (HVPS). The simplified data passing diagram in PDM block with data flow specification represented in **fig.2**.

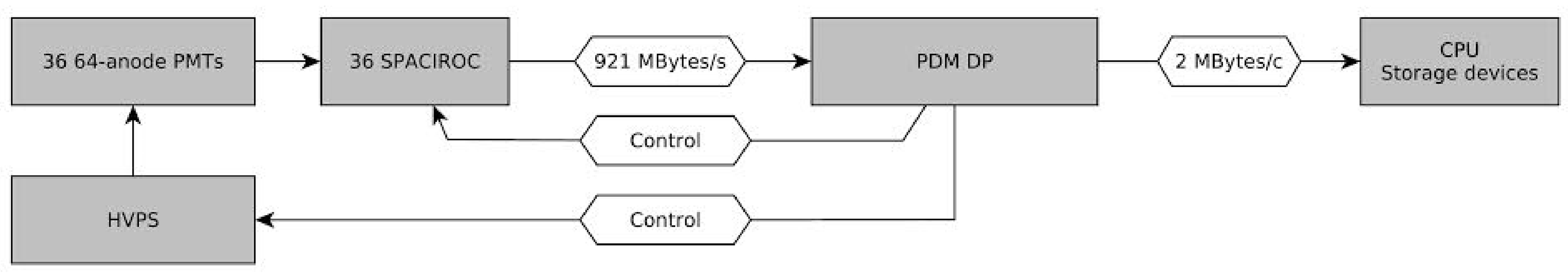


Fig.2 Simplified data passing diagram.

To implement fast data analyses and data transmission the so called System on chip (SoC) which is a composition of FPGA and processing system in one chip was chosen. It allows to realize all algorithms in one chip, simplify the development of the equipment and decrease the total power consumption of the system. PDM DP module has been designed using **Xilinx ZYNQ 7000 chip**. The chip consists of two main parts -- programmable logic (PL) and processing system (PS). The PDM DP uses **external dynamic memory DDR3**, which provides a continuous recording speed of up to 1600 MB/s.

The **PDM DP consists of** three board - ZYNQ board, Cross board and Power board (it can be seen in the right panel of the fig.1). On the ZYNQ board SoC ZYNQ chip, external memory DDR3, physical level Ethernet chip are placed. The Cross board is required for FPGA pins expansion. It contains 3 synchronized Xilinx Artix7 FPGAs which perform data gathering from the ASICs, pixel mapping and data multiplexing. Simplified diagram is presented in **fig.3**.

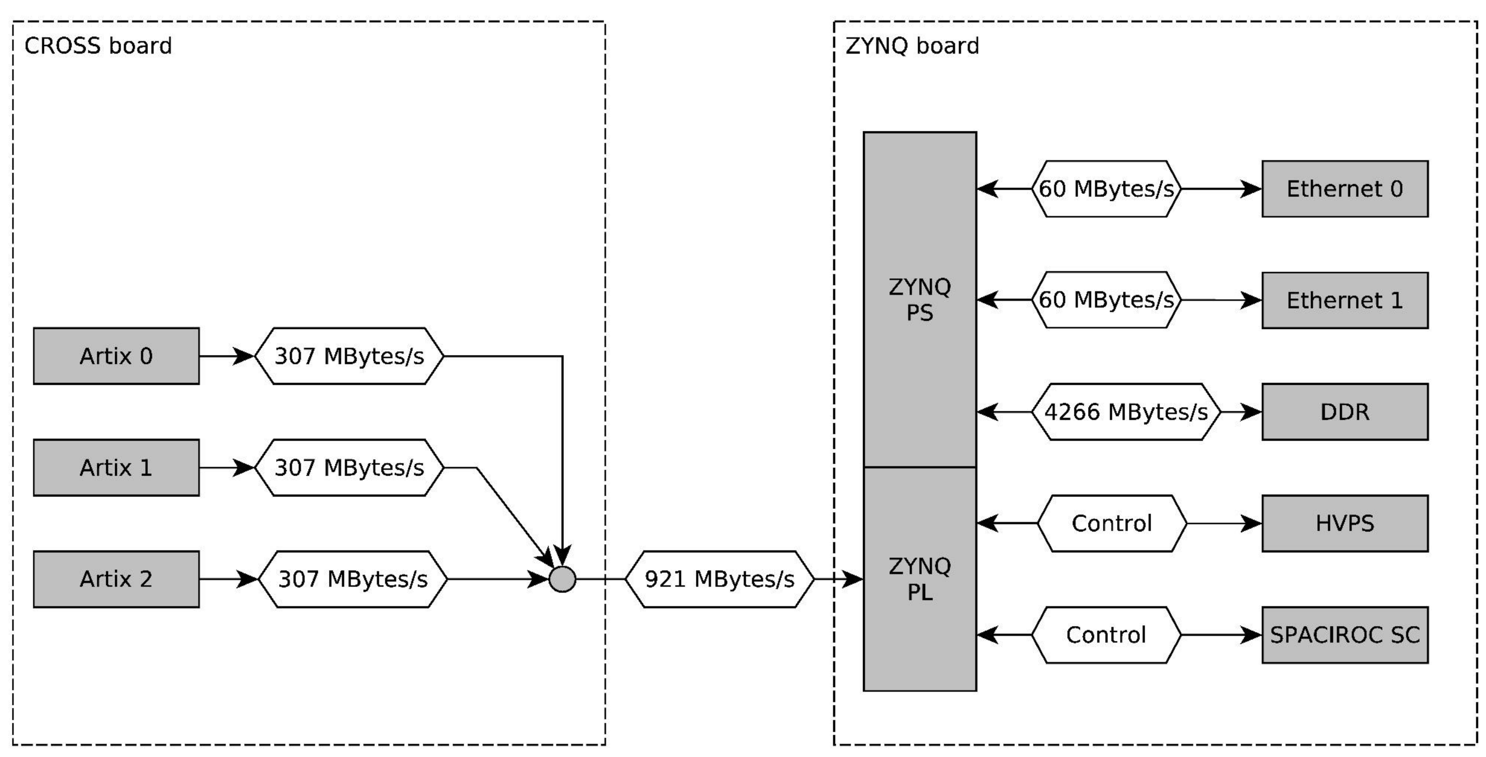


Fig.3

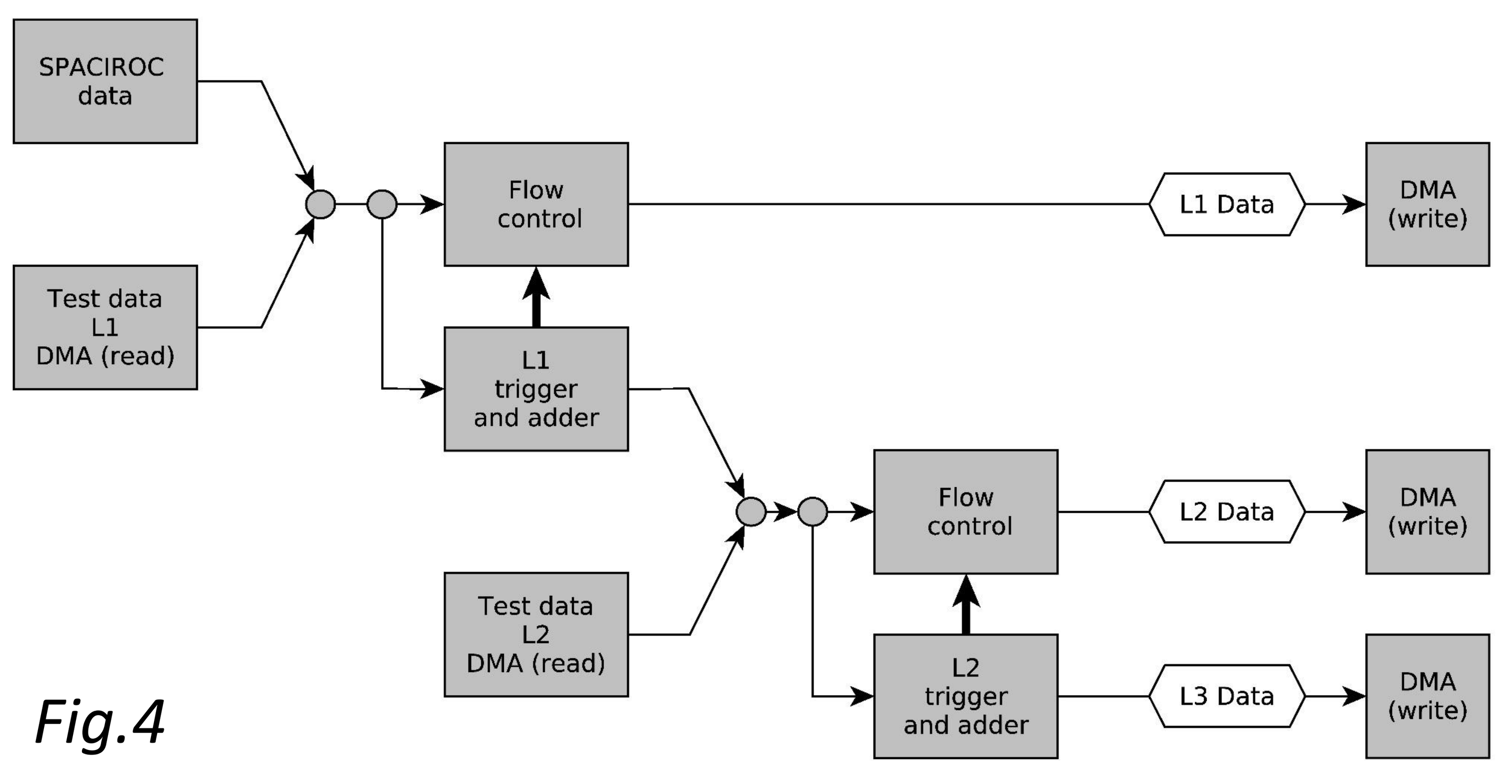


Fig.4

The Mini-EUSO trigger algorithm is implemented in Hardware Description Language (HDL) inside the PL of the ZYNQ board and consists of two levels, L1 and L2, that work with different time resolution. The L1 trigger gives data with a time resolution of 2.5 μs and looks for signal excess on a timescale of 20 μs, as this corresponds to the timescale of EECR like events. The L2 trigger operates with a similar logic, but with a time resolution of 320 μs, well-suited to capturing fast atmospheric events, such as TLEs and lightning. L3 data is a continuous "movie" with 40.96 ms temporal resolution. The data path structure in ZYNQ firmware for Mini-EUSO is shown in **fig.4**.